

**What is claimed is:**

1           1.    A method for filling a uniform mask layer in a trench  
2   of a trench capacitor, comprising:

3           providing a semiconductor substrate, wherein the  
4           semiconductor substrate has a dense trench area and  
5           a less dense trench area with a plurality of trenches  
6           formed in both areas respectively;

7           forming a mask layer covering the semiconductor  
8           substrate, wherein the trenches are filled with the  
9           mask layer;

10          etching the mask layer at an angle until the dense trench  
11          area and the less dense trench area in the  
12          semiconductor substrate are exposed to leave the  
13          mask layer in the trenches; and

14          etching the mask layers in the trenches, and a uniform  
15          thickness of the mask layer in each trench is  
16          achieved.

1           2.    The method for filling a uniform mask layer in a  
2   trench of a trench capacitor of claim 1, wherein the angle  
3   is greater than 45 degrees relative to the normal angle.

1           3.    The method for filling a uniform mask layer in a  
2   trench of a trench capacitor of claim 1, wherein the mask layer  
3   is a photoresist layer.

1           4.    A method for filling a uniform mask layer in a trench  
2   of a trench capacitor of a DRAM, comprising:

3           providing a semiconductor substrate, wherein a first  
4           liner layer and a second liner layer sequentially

5           formed thereon, and the semiconductor substrate has  
6           a dense trench area and a less dense trench area  
7           with a plurality of trenches formed in both areas  
8           respectively;  
9           conformably forming a doped insulating layer covering  
10          the second liner layer and the trenches;  
11          forming a photoresist layer covering the doped insulating  
12          layer and the trenches are filled with the  
13          photoresist layer;  
14          etching the photoresist layer at an angle until the dense  
15          trench area and the less dense trench area in the  
16          semiconductor substrate are exposed to leave the  
17          photoresist layer in the trenches;  
18          etching the photoresist layers in the trenches, and a  
19          uniform thickness of the photoresist layers in each  
20          trench is achieved;  
21          etching the doped insulating layer using the photoresist  
22          layers as etching masks until the exposed doped  
23          insulating layer is removed to leave the doped  
24          insulating layer in the trenches;  
25          removing the photoresist layer; and  
26          diffusing the doped insulating layers to form a plurality  
27          of doped areas in the semiconductor substrate,  
28          wherein the doped areas are substantially the same  
29          in size.

1           5.   The method for filling a uniform mask layer in a  
2           trench of a trench capacitor of claim 4, wherein the first  
3           liner layer is a liner oxide layer.

1           6.    The method for filling a uniform mask layer in a  
2    trench of a trench capacitor of claim 4, wherein the second  
3    liner oxide layer is a liner nitride layer.

1           7.    The method for filling a uniform mask layer in a  
2    trench of a trench capacitor of claim 4, wherein the doped  
3    insulating layer is an ASG layer.

1           8.    The method for filling a uniform mask layer in a  
2    trench of a trench capacitor of claim 4, wherein the angle  
3    is greater than 45 degrees relative to the normal angle.

1           9.    A method for forming a uniform bottom electrode in  
2    a trench of a trench capacitor, comprising:

3           providing a semiconductor substrate, wherein the  
4           semiconductor substrate has a dense trench area and  
5           a less dense trench area with a plurality of trenches  
6           formed in both areas respectively;

7           sequentially forming a first liner layer, a second liner  
8           layer, a mask layer, and a patterned photoresist  
9           layer with a plurality of openings, wherein a portion  
10          of the mask layer is exposed via the openings;

11          sequentially etching the exposed mask layer, the second  
12          liner layer, the first liner layer, and the  
13          semiconductor substrate using the patterned  
14          photoresist layer as an etching mask to form a  
15          plurality of trenches in a dense trench area and  
16          a less dense trench area;

17          sequentially removing the patterned photoresist layer  
18          and the mask layer;

19 conformably forming a doped glass layer covering the  
20 second liner layer and the trenches;  
21 forming a photoresist layer covering the doped glass  
22 layer, and the trenches are filled with the  
23 photoresist layer;  
24 etching the photoresist layer at an angle until the dense  
25 trench area and the less dense trench area in the  
26 semiconductor substrate are exposed to leave the  
27 photoresist layer in the trenches;  
28 etching the photoresist layer to a predetermined depth  
29 in the trenches, and a remaining photoresist layer  
30 is formed;  
31 removing the exposed doped glass layer using the remaining  
32 photoresist layer as a mask;  
33 removing the remaining photoresist layer;  
34 annealing the semiconductor substrate to form an ion doped  
35 area as a bottom electrode in the semiconductor  
36 substrate; and  
37 removing the doped glass.

1 10. The method for forming a uniform bottom electrode  
2 in a trench of a trench capacitor of claim 9, wherein the first  
3 liner layer is a liner oxide layer.

1 11. The method for forming a uniform bottom electrode  
2 in a trench of a trench capacitor of claim 9, wherein the second  
3 liner oxide layer is a liner nitride layer.

1 12. The method for forming a uniform bottom electrode  
2 in a trench of a trench capacitor of claim 9, wherein the mask  
3 layer is a BSG layer.

1           13. The method for forming a uniform bottom electrode  
2           in a trench of a trench capacitor of claim 9, wherein the doped  
3           insulating layer is an ASG layer.

1           14. The method for forming a uniform bottom electrode  
2           in a trench of a trench capacitor of claim 10, wherein the  
3           angle is greater than 45 degrees relative to the normal angle.